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# UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No. MI22-1284

First Inventor or Application Identifier Eugene P. Marsh

Title See 1 in Addendum

Express Mail Label No. EL169866407

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## APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1.  \* Fee Transmittal Form (e.g., PTO/SB/17)  
(Submit an original and a duplicate for fee processing)
2.  Specification [Total Pages 28]  
(preferred arrangement set forth below)
  - Descriptive title of the Invention
  - Cross References to Related Applications
  - Statement Regarding Fed sponsored R & D
  - Reference to Microfiche Appendix
  - Background of the Invention
  - Brief Summary of the Invention
  - Brief Description of the Drawings (if filed)
  - Detailed Description
  - Claim(s)
  - Abstract of the Disclosure
3.  Drawing(s) (35 U.S.C. 113) [Total Sheets 2]
4. Oath or Declaration [Total Pages 2]
  - a.  Newly executed (original or copy)
  - b.  Copy from a prior application (37 C.F.R. § 1.63(d))  
(for continuation/divisional with Box 16 completed)
    - i.  DELETION OF INVENTOR(S)  
Signed statement attached deleting  
inventor(s) named in the prior application,  
see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

\* NOTE FOR ITEMS 1 & 13 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

Assistant Commissioner for Patents  
ADDRESS TO: Box Patent Application  
Washington, DC 20231

5.  Microfiche Computer Program (Appendix)
6. Nucleotide and/or Amino Acid Sequence Submission  
(if applicable, all necessary)
  - a.  Computer Readable Copy
  - b.  Paper Copy (identical to computer copy)
  - c.  Statement verifying identity of above copies

## ACCOMPANYING APPLICATION PARTS

7.  Assignment Papers (cover sheet & document(s))
8.  37 C.F.R. § 3.73(b) Statement  Power of  
(when there is an assignee)  Attorney
9.  English Translation Document (if applicable)
10.  Information Disclosure Statement (IDS)/PTO-1449  Copies of IDS  
Statement (IDS)/PTO-1449  Citations
11.  Preliminary Amendment
12.  Return Receipt Postcard (MPEP 503)  
(Should be specifically itemized)
13.  \* Small Entity Statement(s)  Statement filed in prior application  
(PTO/SB/09-12)  Status still proper and desired
14.  Certified Copy of Priority Document(s)  
(if foreign priority is claimed)
15.  Other: See 2 in Addendum

16. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment:

Continuation  Divisional  Continuation-in-part (CIP)

of prior application No: 09/281,735

Prior application information: Examiner H. Vu

Group / Art Unit: 2811

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

## 17. CORRESPONDENCE ADDRESS

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## 1 IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

2 Priority Application Serial No. .... 09/281,735  
3 Priority Filing Date ..... March 30, 1999  
4 Inventor ..... Eugene P. Marsh  
5 Assignee ..... Micron Technology, Inc.  
6 Priority Group Art Unit ..... 2811  
7 Priority Examiner ..... H. Vu  
Attorney's Docket No. ..... MI22-1284  
Title: Circuitry Comprising Roughened Platinum Layers, Platinum-  
Containing Materials, Capacitors Comprising Roughened  
Platinum Layers, Methods of Forming Roughened Layers of  
Platinum, and Methods of Forming Capacitors

8  
9 **PRELIMINARY AMENDMENT**

10 To: Assistant Commissioner for Patents  
11 Washington, D.C. 20231

12 From: David G. Latwesen (Tel. 509-624-4276; Fax 509-838-3424)  
13 Wells, St. John, Roberts, Gregory & Matkin P.S.  
14 601 W. First Avenue, Suite 1300  
15 Spokane, WA 99201-3828

16 **AMENDMENTS**17 **In the Specification**

18 At p. 1, before the "Technical Field" section, insert

19 **--RELATED PATENT DATA**

20 This patent resulted from a continuation application of U.S. Patent  
21 Application Serial No. 09/281,735, which was filed on March 30, 1999,  
22 which is a divisional application of U.S. Patent Application Serial  
23 No. 09/141,840, which was filed on August 27, 1998--.

1      **In the Claims**

2      Cancel claims 1-56.

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1      **New Claims**

2      57. An integrated circuit comprising hemispherical grain platinum.

4      58. An integrated circuit comprising:

5            a monocrystalline silicon substrate; and

6            a roughened platinum layer over the substrate, the roughened  
7            platinum layer being continuous over an area of the substrate that  
8            comprises at least about  $4 \times 10^6$  square Angstroms and comprising  
9            pedestals that are at least about 300Å tall within the area.

10  
11      59. The circuit of claim 58 wherein the platinum layer comprises  
12            hemispherical grain platinum.

13  
14      60. The circuit of claim 58 wherein the area of the substrate  
15            comprises a square.

16  
17      61. An integrated circuit comprising:  
18            a monocrystalline silicon substrate; and  
19            a roughened platinum layer over the substrate, the roughened  
20            platinum layer having a continuous surface characterized by columnar  
21            pedestals having heights greater than or equal to about one-third of a  
22            total thickness of the platinum layer.

1       62. The circuit of claim 61 wherein the platinum layer has a  
2 thickness of at least about 600Å.

3  
4       63. The circuit of claim 61 wherein the platinum layer has a  
5 thickness of greater than or equal to about 400Å.

6  
7       64. The circuit of claim 61 wherein the platinum layer has a  
8 thickness of greater than or equal to about 100Å.

9  
10       65. The circuit of claim 61 further comprising an adhesion layer  
11 between the platinum layer and the substrate, the adhesion layer  
12 comprising at least one of titanium nitride, iridium, rhodium, ruthenium,  
13 platinum, palladium, osmium, silver, rhodium/platinum alloy,  $\text{IrO}_2$ ,  $\text{RuO}_2$ ,  
14  $\text{RhO}_2$ , or  $\text{OsO}_2$ .

15  
16       66. The circuit of claim 61 wherein the pedestals terminate in  
17 dome-shaped tops.

18  
19       67. The circuit of claim 61 wherein the pedestals terminate in  
20 hemispherical tops.

1           68. A capacitor comprising:

2           a first capacitor electrode over a monocrystalline silicon substrate;

3           a second capacitor electrode;

4           a dielectric layer between the first and second capacitor electrodes;

5           and

6           wherein at least one of the first and second capacitor electrodes  
7           comprises a roughened platinum layer, the roughened platinum layer  
8           having a thickness of from about 400Å to about 1000Å and comprising  
9           pedestals that are at least about 300Å tall.

10  
11           69. The capacitor of claim 68 wherein the roughened platinum  
12           layer comprises hemispherical grain platinum.

13  
14           70. The capacitor of claim 68 wherein the roughened platinum  
15           layer is over a surface and is continuous over an area of the surface  
16           that is at least about  $4 \times 10^6$  square Angstroms.

17  
18           71. The capacitor of claim 70 wherein the area comprises a  
19           square.

1       72. A capacitor comprising:

2           a first capacitor electrode over a monocrystalline silicon substrate;

3           a second capacitor electrode;

4           a dielectric layer between the first and second capacitor electrodes;

5 and

6           wherein at least one of the first and second capacitor electrodes  
7           comprises a roughened platinum layer, the roughened platinum layer  
8           having a continuous surface characterized by columnar pedestals having  
9           heights greater than or equal to about one-third of a total thickness of  
10          the platinum layer.

11

12       73. The capacitor of claim 72 wherein both capacitor electrodes  
13          comprise platinum, but only one of the capacitor electrodes comprises  
14          the roughened platinum layer.

15

16       74. The capacitor of claim 72 wherein both capacitor electrodes  
17          comprise roughened platinum layers.

18

19       75. The circuit of claim 72 wherein the pedestals terminate in  
20          dome-shaped tops.

76. The circuit of claim 72 wherein the pedestals terminate in hemispherical tops.

## REMARKS

Claims 1-56 are canceled, and new claims 57-76 are added.

Claims 57-76 are pending in the application, and Applicant requests examination of such pending claims.

Respectfully submitted,

Dated: 10/19/97

By: John G. Jones B1, D

David G. Latwesen, Ph.D.

Reg. No.: 38,533

EL051032007

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**APPLICATION FOR LETTERS PATENT**

\* \* \* \* \*

CIRCUITRY COMPRISING ROUGHENED  
PLATINUM LAYERS, PLATINUM-CONTAINING  
MATERIALS, CAPACITORS COMPRISING  
ROUGHENED PLATINUM LAYERS, METHODS  
OF FORMING ROUGHENED LAYERS OF  
PLATINUM, AND METHODS OF FORMING  
CAPACITORS

\* \* \* \* \*

INVENTOR  
Eugene P. Marsh

ATTORNEY'S DOCKET NO. MI22-857

1 CIRCUITRY COMPRISING ROUGHENED PLATINUM LAYERS,  
2 PLATINUM-CONTAINING MATERIALS  
3 CAPACITORS COMPRISING ROUGHENED PLATINUM LAYERS,  
4 METHODS OF FORMING ROUGHENED LAYERS OF PLATINUM,  
5 AND METHODS OF FORMING CAPACITORS

6 **TECHNICAL FIELD**

7 The invention pertains to methods of forming and using platinum-  
8 containing materials, and to circuitry incorporating roughened layers of  
9 platinum.

10 **BACKGROUND OF THE INVENTION**

11 Platinum is a candidate for utilization as a conductive material in  
12 advanced semiconductor processing. Platinum can be utilized in an  
13 elemental form, or as an alloy (such as, for example, rhodium/platinum),  
14 and can be deposited onto a substrate by, for example, sputter deposition  
15 or chemical vapor deposition (CVD) methods. Platinum is typically  
16 formed to have a relatively smooth upper surface. Such smooth upper  
17 surface can be advantageous in, for example, applications in which  
18 circuitry is formed over the platinum layer. Specifically, the relatively  
19 smooth surface can provide a substantially planar platform upon which  
20 other circuitry is formed. However, there can be advantages to  
21 incorporating roughened conductive layers into integrated circuitry in  
22 applications where high surface area is desired, as with capacitor  
23

1 electrodes. Accordingly, it would be desirable to develop methods of  
2 forming platinum layers having roughened outer surfaces.

3 In another aspect of the prior art, platinum-comprising materials  
4 are frequently utilized as catalysts in, for example, the petroleum  
5 industry, as well as in, for example, automobile exhaust systems.  
6 Frequently, an efficiency of a catalyst can be improved by enhancing a  
7 surface area of the catalyst. Accordingly, it would be desirable to  
8 develop methods of enhancing surface area of platinum-comprising  
9 materials.

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## SUMMARY OF THE INVENTION

In one aspect, the invention encompasses a method of forming a roughened layer of platinum. A substrate is provided within a reaction chamber. An oxidizing gas is flowed into the reaction chamber, and a platinum precursor is flowed into the chamber. Platinum is deposited from the platinum precursor over the substrate in the presence of the oxidizing gas. A temperature within the chamber is maintained at from about 0°C to less than 300°C during the depositing.

In another aspect, the invention encompasses a circuit comprising a roughened platinum layer over a substrate. The roughened platinum layer has a continuous surface characterized by columnar pedestals.

In yet another aspect, the invention encompasses a platinum catalyst characterized by a continuous outer surface portion of the platinum having a plurality of columnar pedestals that are at least about 400Å tall. The surface portion covers an area that is at least about  $4 \times 10^6$  square Angstroms.

## BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic, fragmentary, cross-sectional view of a semiconductive wafer fragment processed according to a method of the present invention.

1       Fig. 2 is a fragmentary top view of the semiconductor wafer  
2 fragment of Fig. 1.

3       Fig. 3 is a view of the Fig. 1 wafer fragment at a processing step  
4 subsequent to that of Fig. 1.

5       Fig. 4 is a scanning electron microscope (SEM) micrograph of a  
6 platinum film produced by CVD of  $\text{MeCpPt}(\text{Me})_3$ .

7       Fig. 5 is a SEM micrograph of a platinum film produced by CVD  
8 of  $\text{MeCpPt}(\text{Me})_3$  under different conditions than those utilized for  
9 forming the film of Fig. 4.

10

11 **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

12       This disclosure of the invention is submitted in furtherance of the  
13 constitutional purposes of the U.S. Patent Laws "to promote the progress  
14 of science and useful arts" (Article 1, Section 8).

15       The invention encompasses methods of forming platinum layers  
16 having roughened outer surfaces, and methods of incorporating such  
17 layers into capacitor constructions. Fig. 1 shows a semiconductor wafer  
18 fragment 10 at a preliminary processing step of the present invention.  
19 Wafer fragment 10 comprises a substrate 12. Substrate 12 can comprise,  
20 for example, a monocrystalline silicon wafer lightly doped with a  
21 background p-type dopant. To aid in interpretation of the claims that  
22 follow, the term "semiconductive substrate" is defined to mean any  
23 construction comprising semiconductive material, including, but not limited

1 to, bulk semiconductive materials such as a semiconductive wafer (either  
2 alone or in assemblies comprising other materials thereon), and  
3 semiconductive material layers (either alone or in assemblies comprising  
4 other materials). The term "substrate" refers to any supporting  
5 structure, including, but not limited to, the semiconductive substrates  
6 described above.

7 A diffusion region 14 is formed within substrate 12 and defines a  
8 node location to which electrical connection with a storage node of a  
9 capacitor is to be made. Diffusion region 14 can be formed by, for  
10 example, implanting a conductivity enhancing dopant into substrate 12.

11 An adhesion layer 16 is formed over substrate 12 and in electrical  
12 contact with diffusion region 14, and a platinum-comprising layer 18 is  
13 formed over adhesion layer 16. Adhesion layer 16 is provided to  
14 enhance adhesion of platinum-comprising layer 18 to substrate 12. In  
15 other embodiments (not shown) a platinum-comprising layer can be  
16 provided directly onto a silicon surface (either the monocrystalline silicon  
17 surface of substrate 12, or an intervening amorphous or polycrystalline  
18 surface). Such embodiments are less preferred than the shown  
19 embodiment due to difficulties of adequately adhering platinum directly  
20 to silicon.

21 Adhesion layer 16 can comprise, for example, at least one of  
22 titanium nitride, iridium, rhodium, ruthenium, platinum, palladium,  
23 osmium, silver, rhodium/platinum alloy,  $\text{IrO}_2$ ,  $\text{RuO}_2$ ,  $\text{RhO}_2$ , or  $\text{OsO}_2$ .

1 Adhesion layer 16 can be formed by, for example, chemical vapor  
2 deposition, and can be formed to a thickness of, for example, less  
3 than 100Å.

4 Platinum-comprising layer 18 can comprise, for example, elemental  
5 platinum, or a platinum alloy, such as rhodium/platinum alloy. Platinum-  
6 comprising layer 18 is provided to have a roughened outer surface 20.  
7 Such can be accomplished by chemical vapor deposition of platinum-  
8 comprising layer 18 under relatively low temperature conditions, and in  
9 the presence of an oxidizing atmosphere. For instance, a platinum-  
10 comprising layer 18 formed as follows will comprise a roughened outer  
11 surface 20.

12 First, substrate 12 is inserted within a CVD reaction chamber. An  
13 oxidizing gas and a platinum precursor are flowed into the reaction  
14 chamber. Platinum is deposited from the platinum precursor over  
15 substrate 12 in the presence of the oxidizing gas. A temperature within  
16 the reaction chamber is maintained at from about 0°C to less than  
17 300°C during the depositing, and a pressure within the reactor is  
18 preferably maintained at from about 0.5 Torr to about 20 Torr. Suitable  
19 control of the temperature and of a relative flow rate of the oxidizing  
20 gas to the platinum precursor causes deposited platinum layer 18 to have  
21 a roughened outer surface 20. The platinum precursor is flowed into  
22 the reaction chamber in a carrier gas, such as, for example, a gas known  
23 to be generally inert to reaction with platinum precursor materials, such

1 as, for example, helium or argon. The platinum precursor can comprise,  
2 for example, at least one of  $\text{MeCpPtMe}_3$ ,  $\text{CpPtMe}_3$ ,  $\text{Pt}(\text{acetylacetone})_2$ ,  
3  $\text{Pt}(\text{PF}_3)_4$ ,  $\text{Pt}(\text{CO})_2\text{Cl}_2$ ,  $\text{cis-}[\text{PtMe}_2(\text{MeNC})_2]$ , or platinum  
4 hexafluoroacetylacetone; wherein Cp is a cyclopentadienyl group and Me  
5 is a methyl group. The oxidizing gas can comprise, for example, at least  
6 one of  $\text{O}_2$ ,  $\text{N}_2\text{O}$ ,  $\text{SO}_3$ ,  $\text{O}_3$ ,  $\text{H}_2\text{O}_2$ , or  $\text{NO}_x$ , wherein x has a value of  
7 from 1 to 3. In embodiments wherein platinum layer 18 comprises a  
8 platinum/metal alloy, at least one other metal precursor can be flowed  
9 into the reaction chamber to deposit the platinum as an alloy of the  
10 platinum and the at least one other metal. The at least one other  
11 metal precursor can comprise, for example, a precursor of rhodium,  
12 iridium, ruthenium, palladium, osmium, and/or silver.

13 The oxidizing gas can assist in deposition of platinum from the  
14 platinum-comprising precursor by oxidizing carbon from the precursor  
15 during deposition of the platinum. Also, the oxidizing gas can influence  
16 a deposition rate of a platinum-comprising layer. Specifically, a greater  
17 rate of flow of the oxidizing gas relative to the flow of the platinum  
18 precursor can lead to faster deposition of the platinum-comprising layer.  
19 The rate of flow of platinum precursor is influenced by a rate of flow  
20 of carrier gas through a liquid organic precursor solution, and by a  
21 temperature of the precursor solution. In preferred embodiments of the  
22 invention, a carrier gas will be flowed through a liquid organic precursor  
23 solution at a rate of from about 2 sccm to about 1000 sccm and more

1 preferably at less than or equal to about 30 sccm. In such preferred  
2 embodiments, the oxidizing gas will be flowed at a flow rate of at least  
3 about 50 sccm. The organic precursor will preferably be at a  
4 temperature of from about 0°C to about 100°C, and more preferably  
5 from about 30°C to about 50°C.

6 A rate of growth of platinum-comprising layer within the reaction  
7 chamber is also influenced by a temperature of the substrate.  
8 Specifically, if platinum is deposited under conditions wherein the  
9 temperature of the substrate is maintained at from about 220°C to less  
10 than 300°C, the platinum will deposit at a rate of about 600Å in  
11 about 30 seconds. If a temperature of the substrate is reduced to below  
12 about 210°C, a rate of deposition of platinum will decrease considerably.  
13 It is preferred that a deposition time for a 600Å thick platinum-  
14 comprising layer be less than or equal to about 40 seconds to maintain  
15 efficiency of a production process. Accordingly, it is preferred that the  
16 temperature of the substrate be maintained at above about 210°C, and  
17 preferably at from greater than or equal to about 220°C during  
18 deposition of the platinum-comprising layer within the reaction chamber.

19 It is also found that if a temperature is greater than 300°C and  
20 less than about 350°C, a deposited platinum layer will have a smooth  
21 outer surface, rather than a desired roughened outer surface. Further,  
22 if the temperature of the substrate exceeds about 400°C, a deposited  
23 platinum surface will have holes extending to a surface underlying the

1 platinum surface, rather than being a continuous surface overlying a  
2 substrate. Accordingly, it is preferred that the temperature of the  
3 substrate be well below 400°C, more preferred that the temperature be  
4 below 300°C, and even more preferred that the temperature be less than  
5 or equal to about 280°C. In preferred embodiments of the present  
6 invention, the temperature of the substrate will be maintained at from  
7 about 220°C to about 280°C, whereupon it is found that a platinum  
8 layer having a roughened outer surface can be deposited to a thickness  
9 of about 600Å in about 30 seconds.

10 Platinum layer 18 is preferably deposited to a thickness of at least  
11 about 400Å to avoid having surface anomalies (such as crevices or holes)  
12 that extend entirely through layer 18 to an underlying layer, and is  
13 preferably deposited to a thickness of at least about 600Å. However, in  
14 some embodiments holes extending entirely through layer 18 will be of  
15 little or no consequence in semiconductor circuitry ultimately formed  
16 from layer 18. Such embodiments can include, for example, embodiments  
17 wherein adhesion layer 16 is provided beneath platinum-comprising  
18 layer 18. Accordingly, in embodiments wherein platinum layer 18 is  
19 provided over an adhesion layer 16, it can be preferred to provide  
20 platinum layer 18 to a thickness of less than 400Å because of space  
21 limitations due to the close packing of capacitors. Also, in embodiments  
22 in which platinum layer 18 is utilized in forming circuitry having tight  
23 spacing requirements it can be preferred to form layer 18 to be

1 relatively thin. For instance, in some capacitor constructions it can be  
2 desired to form layer 18 to be less than or equal to about 1000Å, and  
3 more preferred to form layer 18 to be from about 300Å to about 400Å  
4 to avoid electrical contact between adjacent capacitor structures.

5 A fragmentary top view of wafer fragment 10 is shown in Fig. 2.  
6 Layer 18 is preferably a continuous layer (defined as a layer without  
7 cavities extending therethrough to an underlying layer -- such as the  
8 underlying layer 16 of Fig. 2) across its entirety. Alternatively, some  
9 portion of layer 18 is continuous. For example, consider an application  
10 where layer 18 overlies and contacts a conductive layer to form a circuit  
11 device comprising both layer 18 and the underlying conductive layer. In  
12 such applications, it is generally still desired that a substantial portion  
13 of layer 18 be continuous to, for example, maintain a uniform electrical  
14 contact between layer 18 and the underlying conductive layer. Such  
15 substantial portion will preferably cover a surface area of at least about  
16  $4 \times 10^6$  square Angstroms. A surface area of about  $4 \times 10^6$  square  
17 Angstroms is illustrated in Fig. 3 as a square 50 having sides of about  
18 2000 Angstroms.

19 Fig. 3 illustrates an embodiment wherein platinum-comprising  
20 layer 18 is incorporated into a capacitor construction 30 as a storage  
21 node. Specifically, a dielectric layer 22 and a capacitor electrode 24 are  
22 provided over platinum-comprising layer 18 to form capacitor  
23 construction 30. Dielectric layer 22 can comprise one or more of silicon

oxide or silicon nitride, or it can comprise other dielectric materials, such as, for example, tantalum pentoxide, or  $\text{BaSrTiO}_3$ . Capacitor electrode 24 can comprise, for example, TiN, conductively doped silicon (such as polysilicon), or a metal, such as, for example, platinum. In embodiments wherein capacitor electrode 24 comprises platinum, capacitor electrode 24 can be formed by chemical vapor deposition over dielectric layer 22. The chemical vapor deposition can be conducted either to form upper electrode 24 with a relatively smooth upper surface, or to form upper electrode 24 with a relatively rough upper surface. If capacitor electrode 24 is to be formed of platinum with a relatively smooth upper surface, it can be chemical vapor deposited in a reaction chamber with a temperature maintained at above about  $300^\circ\text{ C}$  and/or with an oxidizing gas flow rate of less than 50 sccm and a carrier gas flow rate of greater than 30 sccm. Also, any platinum comprised by capacitor electrode 24 can be in the form of elemental platinum, or an alloy, such as, for example, rhodium/platinum alloy.

As shown, layer 18 has a rough outer surface and layers 22 and 24 are conformal to the rough outer surface of layer 18.

Figs. 4 and 5 illustrate scanning electron microscope (SEM) micrographs of platinum films produced by CVD of  $\text{MeCpPt}(\text{Me})_3$ . Fig. 4 illustrates a surface produced within a reaction chamber in a time of about 6 minutes, wherein a temperature in the chamber was about  $215^\circ\text{C}$ , a pressure was about 5 Torr, a flow rate of carrier gas

(He, with a pressure at the carrier gas bubbler of about 6 Torr) was about 5 sccm, and a flow rate of oxidizing gas (O<sub>2</sub>) was about 50 sccm. The platinum surface formed comprises pedestals characteristic of columnar growth. The columnar pedestals terminate in dome-shaped (substantially hemispherical) tops. It can be advantageous to have substantially hemispherical tops, rather than tops having sharp edges, in forming capacitor constructions or other electronic circuitry from a deposited platinum layer. Specifically, the relatively rounded hemispherical surfaces can create relatively uniform electric fields at the surface of a deposited platinum layer. In contrast, if sharp edges were present, the sharp edges could form loci for high electric fields, and lead to leakage of electric current across the capacitor. The platinum layer illustrated in Fig. 4 can be referred to as "hemispherical grain" platinum to indicate a structure largely analogous to a material known in the art as hemispherical grain polysilicon.

The platinum layer of Fig. 4 is characterized by columnar pedestals generally having heights greater than or equal to about one-third of a total thickness of the platinum layer. Many of the pedestals shown in Fig. 4 have a height approximately equal to a thickness of the deposited platinum layer. Accordingly, if the deposited platinum layer has a thickness of about 600Å, the individual pedestals can have a thickness approaching 600Å. Such is only an approximation to the size of the pedestals as it is found that some of the pedestals will grow from

surfaces of other pedestals, and some of the pedestals will grow less vertically than other pedestals. An average diameter of the pedestals is about 200Å, and the pedestals are generally closely packed (i.e., the pedestals generally touch other pedestals and many pedestals fuse with other pedestals), but the distribution of the pedestals is typically not a close-packed structure (i.e., a structure wherein all the pedestals are tightly packed in, for example, an hexagonal type arrangement to form a maximum number of pedestals on a given surface). The columnar growth illustrated in Fig. 4 is found not to occur if a temperature within a CVD reaction chamber is above 300°C.

Fig. 5 illustrates a surface produced on a platinum film within a reaction chamber in a time of about 150 seconds, wherein a temperature in the chamber was 300°C, a pressure was about 0.5 Torr, a flow rate of carrier gas (He, with a pressure at the carrier gas bubbler of about 6 Torr) was about 30 sccm, and a flow rate of oxidizing gas (O<sub>2</sub>) was about 10 sccm. The platinum layer deposited under the Fig. 5 conditions has a much smoother surface than that deposited under the Fig. 4 conditions. Figs 4 and 5 together evidence that it is possible to control a grain structure of a surface of a chemical vapor deposited platinum layer by controlling process parameters of a chemical vapor deposition reaction chamber.

Although the invention has been described with application to formation of a capacitor structure, it is to be understood that the

1 invention can be utilized in a number of other applications as well. For  
2 instance, a platinum layer having a roughened surface can be utilized for  
3 formation of catalysts.

4 In compliance with the statute, the invention has been described  
5 in language more or less specific as to structural and methodical  
6 features. It is to be understood, however, that the invention is not  
7 limited to the specific features shown and described, since the means  
8 herein disclosed comprise preferred forms of putting the invention into  
9 effect. The invention is, therefore, claimed in any of its forms or  
10 modifications within the proper scope of the appended claims  
11 appropriately interpreted in accordance with the doctrine of equivalents.

1        CLAIMS:

2        1. A method of forming a roughened layer of platinum,  
3        comprising:

4                providing a substrate within a reaction chamber;  
5                flowing an oxidizing gas into the reaction chamber;  
6                flowing a platinum precursor into the reaction chamber and  
7        depositing platinum from the platinum precursor over the substrate in  
8        the presence of the oxidizing gas; and  
9                maintaining a temperature within the reaction chamber at from  
10        about 0°C to less than 300°C during the depositing.

11  
12        2. The method of claim 1 further comprising providing a  
13        reactant in contact with the roughened layer of platinum and utilizing  
14        the platinum to catalyze a conversion of the reactant to a product.

15  
16        3. The method of claim 1 wherein the flowing the platinum  
17        precursor comprises flowing a carrier gas carrying the platinum precursor,  
18        the carrier gas being flowed at a rate of no greater than about 30 sccm  
19        and the oxidizing gas being flowed at a rate of at least about 50 sccm.

1           4. The method of claim 1 wherein the oxidizing gas comprises  
2           at least one of O<sub>2</sub>, N<sub>2</sub>O, SO<sub>3</sub>, O<sub>3</sub>, H<sub>2</sub>O<sub>2</sub>, or NO<sub>x</sub>, wherein x has a value  
3           of from 1 to 3.

4  
5           5. The method of claim 1 wherein the platinum precursor  
6           comprises at least one of MeCpPtMe<sub>3</sub>, CpPtMe<sub>3</sub>, Pt(acetylacetonate)<sub>2</sub>,  
7           Pt(PF<sub>3</sub>)<sub>4</sub>, Pt(CO)<sub>2</sub>Cl<sub>2</sub>, cis-[PtMe<sub>2</sub>(MeNC)<sub>2</sub>], or platinum  
8           hexafluoroacetylacetone.

9  
10          6. The method of claim 1 wherein the maintaining comprises  
11          maintaining the temperature at from about 200°C to less than 300°C.

12  
13          7. The method of claim 1 wherein the maintaining comprises  
14          maintaining the temperature at from about 220°C to about 280°C.

15  
16          8. The method of claim 1 further comprising forming an  
17          adhesion layer over the substrate and depositing the platinum onto the  
18          adhesion layer.

1       9. The method of claim 8 wherein the adhesion layer comprises  
2       at least one of titanium nitride, iridium, rhodium, ruthenium, platinum,  
3       palladium, osmium, silver, rhodium/platinum alloy,  $\text{IrO}_2$ ,  $\text{RuO}_2$ ,  $\text{RhO}_2$ , or  
4        $\text{OsO}_2$ .

5  
6       10. The method of claim 1 further comprising flowing at least  
7       one other metal precursor into the chamber in addition to the platinum  
8       precursor, and wherein the platinum is deposited as an alloy of platinum  
9       and the at least one other metal.

10  
11       11. The method of claim 1 further comprising flowing a second  
12       metal precursor into the chamber and wherein the platinum is deposited  
13       as an alloy of platinum and the second metal.

14  
15       12. The method of claim 11 wherein the second metal is  
16       rhodium, iridium, ruthenium, palladium, osmium, or silver.

17  
18       13. The method of claim 1 wherein the platinum is deposited to  
19       a thickness of at least about 400 $\text{\AA}$ .

1           14. The method of claim 1 wherein the maintaining comprises  
2           maintaining the temperature at from about 200°C to less than 300°C,  
3           and wherein the platinum is deposited to a thickness of at least  
4           about 600Å in a time of less than about 40 seconds.

5

6           15. A method of forming a roughened layer of platinum,  
7           comprising:

8           providing a substrate within a reaction chamber;

9           flowing an oxidizing gas into the reaction chamber;

10           flowing a platinum precursor into the chamber and depositing  
11           platinum from the platinum precursor over the substrate in the presence  
12           of the oxidizing gas;

13           maintaining a temperature within the chamber at from about 0°C  
14           to less than or equal to about 280°C during the depositing, the  
15           deposited platinum having a rougher surface than it would have if the  
16           temperature were 300°C or greater during the depositing.

17

18           16. The method of claim 15 wherein the deposited platinum  
19           forms a continuous layer over a surface area that is at least  $4 \times 10^6$   
20           square Angstroms.

1        17. The method of claim 15 wherein the deposited platinum is  
2        hemispherical grain platinum.

3

4        18. A method of forming a capacitor, comprising:  
5        providing a substrate within a reaction chamber;  
6        flowing a first oxidizing gas into the reaction chamber;  
7        flowing a first platinum precursor into the chamber and depositing  
8        platinum from the first platinum precursor over the substrate in the  
9        presence of the first oxidizing gas while maintaining a temperature within  
10      the chamber at from about 0°C to less than 300°C, and providing the  
11      deposited platinum into a first capacitor electrode;  
12      forming a second capacitor electrode proximate the first capacitor  
13      electrode; and  
14      forming a dielectric layer proximate the first capacitor electrode,  
15      the dielectric layer being between the first and second capacitor  
16      electrodes.

17

18        19. The method of claim 18 wherein the flowing the first  
19      platinum precursor comprises flowing a carrier gas carrying the platinum  
20      precursor, the carrier gas being flowed at a rate no greater than  
21      30 sccm and the first oxidizing gas being flowed at a rate of at least 50  
22      sccm.

1           20. The method of claim 18 wherein the forming the second  
2 capacitor electrode comprises depositing platinum from a second platinum  
3 precursor in the presence of a second oxidizing gas.

4

5           21. The method of claim 20 wherein the second platinum  
6 precursor is the same as the first platinum precursor.

7

8           22. The method of claim 20 wherein the second oxidizing gas is  
9 the same as the first oxidizing gas.

10

11          23. The method of claim 20 further comprising flowing a second  
12 metal precursor into the chamber with the first platinum precursor, and  
13 wherein the platinum is deposited as an alloy of platinum and the  
14 second metal.

15

16          24. The method of claim 23 wherein the second metal is  
17 rhodium, iridium, ruthenium, palladium, osmium, or silver.

18

19          25. The method of claim 18 further comprising forming an  
20 adhesion layer over the substrate and depositing the platinum onto the  
21 adhesion layer.

1        26. The method of claim 25 wherein the adhesion layer  
2        comprises at least one of titanium nitride, iridium, rhodium, ruthenium,  
3        platinum, palladium, osmium, silver, rhodium/platinum alloy,  $\text{IrO}_2$ ,  $\text{RuO}_2$ ,  
4         $\text{RhO}_2$ , or  $\text{OsO}_2$ .

5  
6        27. The method of claim 18 wherein the maintaining comprises  
7        maintaining the temperature at from about 200°C to less than 300°C.

8  
9        28. The method of claim 18 wherein the maintaining comprises  
10        maintaining the temperature at from about 220°C to about 280°C.

11  
12        29. A circuit comprising:  
13            a semiconductive substrate; and  
14            a roughened platinum layer over the substrate, the roughened  
15            platinum layer comprising hemispherical grain platinum.

16  
17        30. A circuit comprising:  
18            a semiconductive substrate; and  
19            a roughened platinum layer over the substrate, the roughened  
20            platinum layer being continuous over an area of the substrate that  
21            comprises at least about  $4 \times 10^6$  square Angstroms and comprising  
22            pedestals that are at least about 300Å tall within the area.

1           31. The circuit of claim 30 wherein the platinum layer comprises  
2           hemispherical grain platinum.

3  
4           32. The circuit of claim 30 wherein the area of the substrate  
5           comprises a square.

6  
7           33. A circuit comprising:  
8           a semiconductive substrate; and  
9           a roughened platinum layer over the substrate, the roughened  
10          platinum layer having a continuous surface characterized by columnar  
11          pedestals having heights greater than or equal to about one-third of a  
12          total thickness of the platinum layer.

13  
14          34. The circuit of claim 33 wherein the platinum layer has a  
15          thickness of at least about 600Å.

16  
17          35. The circuit of claim 33 wherein the platinum layer has a  
18          thickness of greater than or equal to about 400Å.

19  
20          36. The circuit of claim 33 wherein the platinum layer has a  
21          thickness of greater than or equal to about 100Å.

1       37. The circuit of claim 33 further comprising an adhesion layer  
2       between the platinum layer and the substrate, the adhesion layer  
3       comprising at least one of titanium nitride, iridium, rhodium, ruthenium,  
4       platinum, palladium, osmium, silver, rhodium/platinum alloy,  $\text{IrO}_2$ ,  $\text{RuO}_2$ ,  
5        $\text{RhO}_2$ , or  $\text{OsO}_2$ .

6

7       38. The circuit of claim 33 wherein the pedestals terminate in  
8       dome-shaped tops.

9

10      39. The circuit of claim 33 wherein the pedestals terminate in  
11      hemispherical tops.

12

13      40. A capacitor comprising:  
14        a first capacitor electrode;  
15        a second capacitor electrode;  
16        a dielectric layer between the first and second capacitor electrodes;  
17        and

18        wherein at least one of the first and second capacitor electrodes  
19        comprises a roughened platinum layer, the roughened platinum layer  
20        having a thickness of from about 400Å to about 1000Å and comprising  
21        pedestals that are at least about 300Å tall.

1           41. The capacitor of claim 40 wherein the roughened platinum  
2           layer comprises hemispherical grain platinum.

3  
4           42. The capacitor of claim 40 wherein the roughened platinum  
5           layer is over a surface and is continuous over an area of the surface  
6           that is at least about  $4 \times 10^6$  square Angstroms.

7  
8           43. The capacitor of claim 42 wherein the area comprises a  
9           square.

10  
11          44. A capacitor comprising:  
12           a first capacitor electrode;  
13           a second capacitor electrode;  
14           a dielectric layer between the first and second capacitor electrodes;  
15           and

16           wherein at least one of the first and second capacitor electrodes  
17           comprises a roughened platinum layer, the roughened platinum layer  
18           having a continuous surface characterized by columnar pedestals having  
19           heights greater than or equal to about one-third of a total thickness of  
20           the platinum layer.

1           45. The capacitor of claim 44 wherein both capacitor electrodes  
2 comprise platinum, but only one of the capacitor electrodes comprises  
3 the roughened platinum layer.

4

5           46. The capacitor of claim 44 wherein both capacitor electrodes  
6 comprise roughened platinum layers.

7

8           47. The circuit of claim 44 wherein the pedestals terminate in  
9 dome-shaped tops.

10

11           48. The circuit of claim 44 wherein the pedestals terminate in  
12 hemispherical tops.

13

14           49. A platinum-containing material, comprising:  
15            a substrate; and  
16            a roughened platinum layer over the substrate, the roughened  
17            platinum layer having a continuous surface characterized by columnar  
18            pedestals having heights greater than or equal to about one-third of a  
19            total thickness of the platinum layer.

20

21           50. The material of claim 49 wherein the pedestals terminate in  
22 dome-shaped tops.

1           51. The material of claim 49 wherein the pedestals terminate in  
2           hemispherical tops.

3

4           52. A reaction catalyst comprising hemispherical grain platinum.

5

6           53. A reaction catalyst characterized by an outer surface portion  
7           of platinum comprising a plurality of columnar pedestals that are at least  
8           about 100Å tall.

9

10          54. The catalyst of claim 53 wherein the columnar pedestals are  
11          at least about 400Å tall.

12

13          55. The catalyst of claim 53 wherein the platinum comprises  
14          hemispherical grain platinum.

15

16          56. The catalyst of claim 53 wherein the surface portion is  
17          continuous over a substrate and covers an area of the substrate that is  
18          at least about  $4 \times 10^6$  square Angstroms.

1            **ABSTRACT OF THE DISCLOSURE**

2            In one aspect, the invention includes a method of forming a  
3            roughened layer of platinum, comprising: a) providing a substrate within  
4            a reaction chamber; b) flowing an oxidizing gas into the reaction  
5            chamber; c) flowing a platinum precursor into the reaction chamber and  
6            depositing platinum from the platinum precursor over the substrate in  
7            the presence of the oxidizing gas; and d) maintaining a temperature  
8            within the reaction chamber at from about 0°C to less than 300°C  
9            during the depositing. In another aspect, the invention includes a  
10           platinum-containing material, comprising: a) a substrate; and b) a  
11           roughened platinum layer over the substrate, the roughened platinum  
12           layer having a continuous surface characterized by columnar pedestals  
13           having heights greater than or equal to about one-third of a total  
14           thickness of the platinum layer.

15

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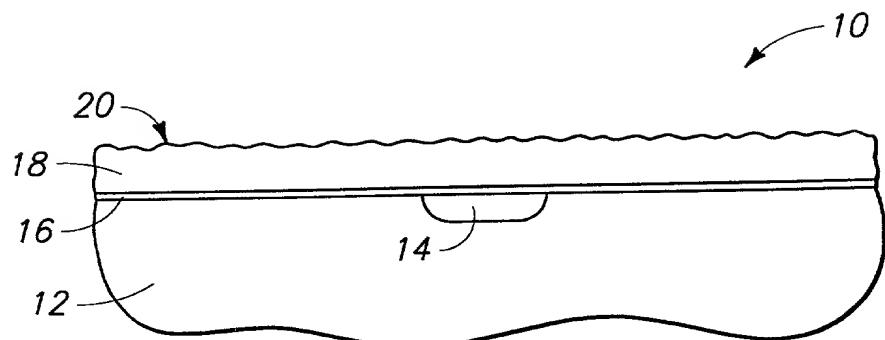
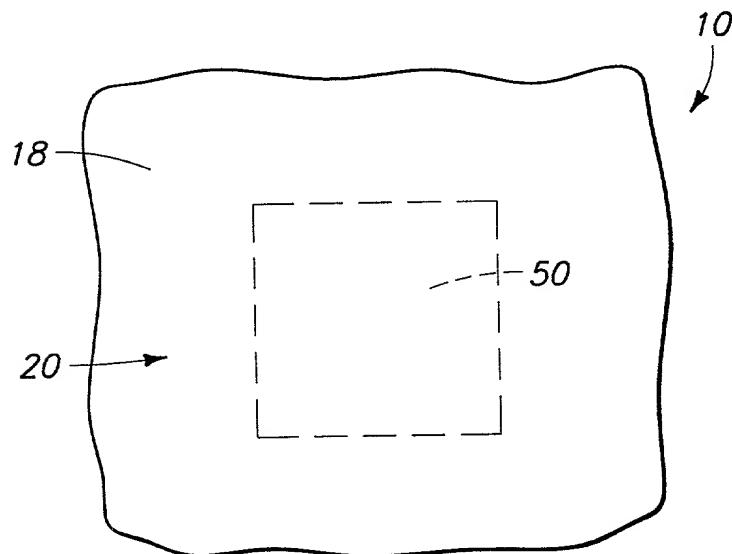
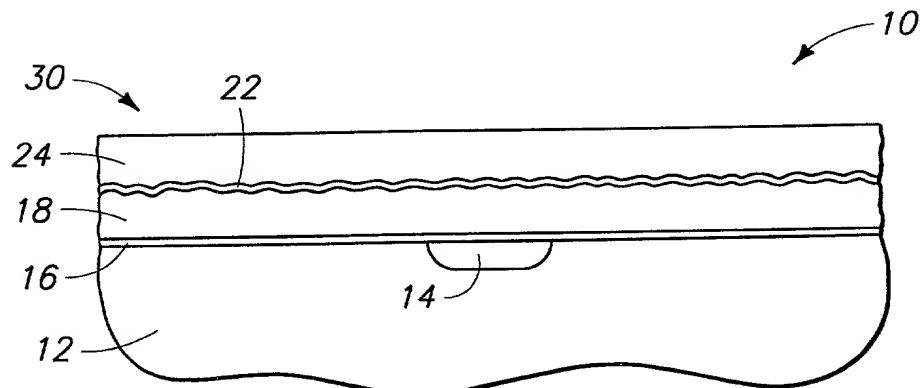
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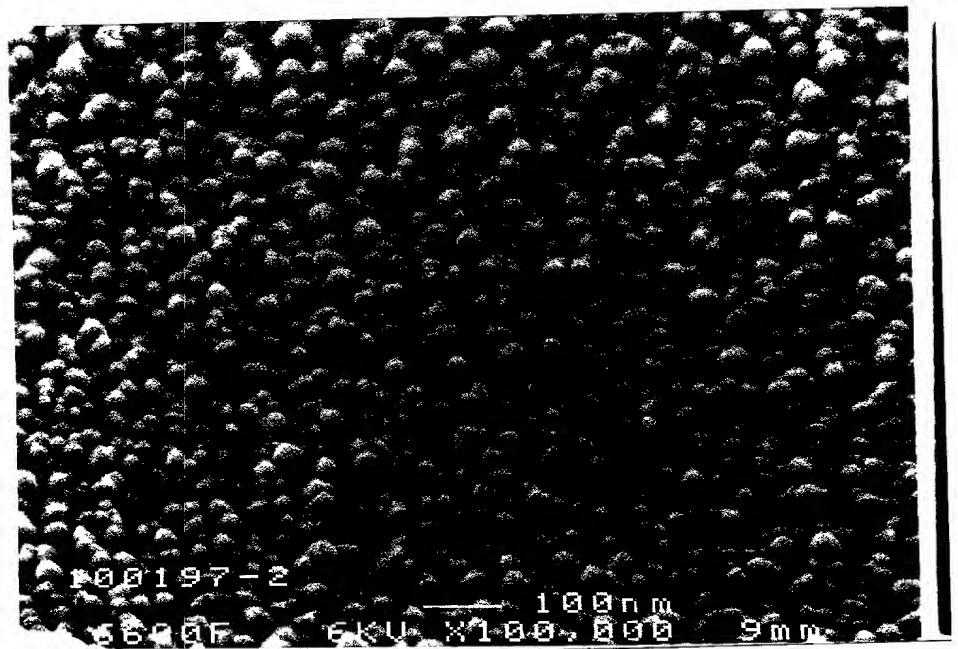
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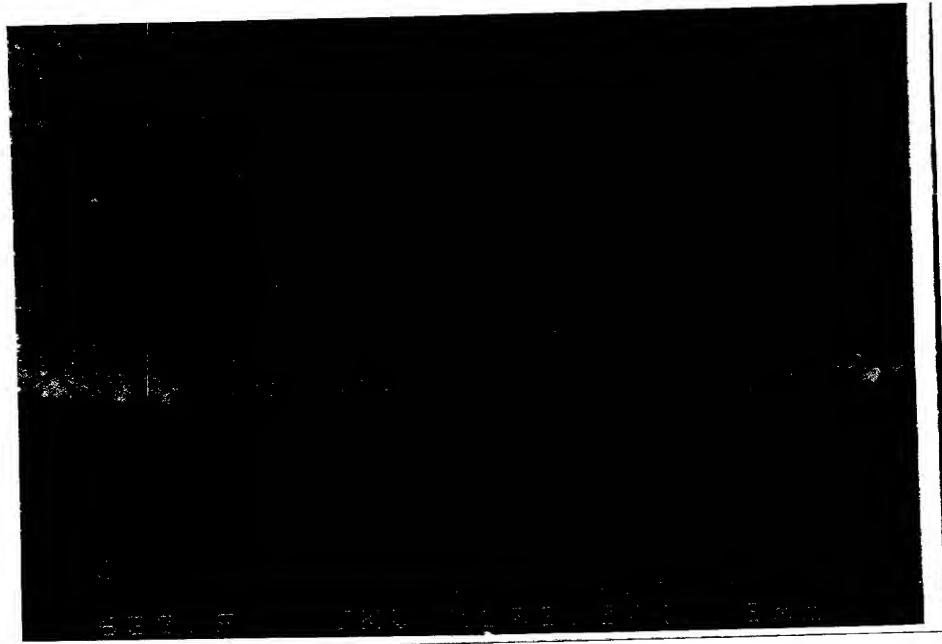
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FIG. II AFIG. II BFIG. II C

2/2



EEG 4



EEG 5

## Addendum

1. Circuitry Comprising Roughened Platinum Layers, Platinum-Containing Materials, Capacitors Comprising Roughened Platinum Layers, Methods of Forming Roughened Layers of Platinum, and Methods of Forming Capacitors
2. - Petition to Accept Photograph(s) as Drawing(s)  
- 1 set of photographs

1                    **DECLARATION OF SOLE INVENTOR FOR PATENT APPLICATION**

2                    As the below named inventor, I hereby declare that:

3                    My residence, post office address and citizenship are as stated  
4                    below next to my name.

5                    I believe I am the original, first and sole inventor of the subject  
6                    matter which is claimed and for which a patent is sought on the  
7                    invention entitled: Circuitry Comprising Roughened Platinum Layers,  
8                    Platinum-Containing Materials, Capacitors Comprising Roughened Platinum  
9                    Layers, Methods Of Forming Roughened Layers Of Platinum, And  
10                   Methods Of Forming Capacitors, the specification of which is attached  
11                   hereto.

12                   I hereby state that I have reviewed and understand the contents  
13                   of the above-identified specification, including the claims.

14                   I acknowledge the duty to disclose information known to me to  
15                   be material to patentability as defined in Title 37, Code of Federal  
16                   Regulations §1.56.

17                   **PRIOR FOREIGN APPLICATIONS:**

18                   I hereby state that no applications for foreign patents or inventor's  
19                   certificates have been filed prior to the date of execution of this  
20                   declaration.

21                   I hereby declare that all statements made herein of my own  
22                   knowledge are true and that all statements made on information and  
23                   belief are believed to be true; and further that these statements were  
24                   made with the knowledge that willful false statements and the like so

1 made are punishable by fine or imprisonment, or both, under  
2 Section 1001 of Title 18 of the United States Code and that such willful  
3 false statement may jeopardize the validity of the application or any  
4 patent issued therefrom.

5 \* \* \* \* \*

6 Full name of sole inventor: Eugene P. Marsh

7 Inventor's Signature: Eugene P. Marsh

8 Date: 8/24/98

9 Residence: Boise, Idaho

10 Citizenship: U.S.

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